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PATENT APPLICATION

ATTORNEY DOCKET NO. 10001844-1

Inventor(s): Lowell E. Kolb

Application No.: 09/813,257

Filing Date: March 19, 2001

Confirmation No.: 2624

Examiner: Tuan T. Dinh

Group Art Unit: 2827

Title: Filler Material and Pretreatment Of A Printed Circuit Board (As Amended)

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Transmitted herewith is/are the following in the above-identified application:

- ☐ Response/Amendment
- ☐ New fee as calculated below
- ☐ No additional fee
- ☒ Other Response to Notice of Non-Compliant Appeal Brief dated 11-28-06 Fee$____
- ☐ Petition to extend time to respond
- ☐ Supplemental Declaration

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY

(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS		MINUS		= 0	X $50	$ 0
INDEP. CLAIMS		MINUS		= 0	X $200	$ 0
☐ FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $360	$ 0
EXTENSION FEE	☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590		$ 0
					OTHER FEES	$
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

Charge $ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

Date of Deposit:

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Signature: _____

Respectfully submitted,

Lowell E. Kolb

By _____

Michael G. Verga, Esq.

Attorney/Agent for Applicant(s)

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Date : December 21, 2006

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PATENT

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In the Matter of the Application of:	Lowell E. Kolb
Serial No.:	09/813,257
Filed:	March 19, 2001
Entitled:	FILLER MATERIAL AND PRETREATMENT OF PRINTED CIRCUIT BOARD COMPONENTS TO FACILITATE APPLICATION OF A CONFORMAL EMI SHIELD
Docket No.:	10001844-1

Group Art Unit: 2841
Examiner: Tuan T. Dinh

Mail Stop: Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

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I. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company of Fort Collins, Colorado. Hewlett-Packard Development Company derives its rights in this application by virtue of assignment of the application by the inventors to Hewlett-Packard Company and the subsequent assignment of the application to Hewlett-Packard Development Company.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1 and 3-17 are currently pending in the present application, Application Number 09/813,257. Claims 1 and 3-17 have been at least twice rejected and, therefore, are subject to appeal.

IV. STATUS OF AMENDMENTS

All Amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Aspects and embodiments of the present invention are directed to a printed circuit board (304) comprising a printed wiring board (202) with at least one component mounted thereon.

One aspect of the invention is directed to a printed circuit board (304) comprising: a printed wiring board (202); a component (302) mounted on the printed wiring board, wherein the printed circuit board (304) has a volume of space (910A, 910B, 910C) bounded by at least one of a body of the component (206), a lead (208) of the component, and said printed wiring board (202), wherein said volume of space has at least one opening on the surface of the printed circuit board; and an electrically non-conductive filler material (902) disposed on the surface of the printed circuit board (304) so as to bridge across the at least one opening of the volume of space to render the volume of space substantially inaccessible to subsequently-applied coatings. *(See,* Applicant's application, pg. 31, ln. 9 to 33, ln. 30.)

Another aspect of the invention is directed to a printed circuit board (304) comprising: a printed wiring board (202); a plurality of components (302) each mounted on said printed wiring board (202), wherein the printed circuit board (304) has at least one volume of space (910A, 910B, 910C) bounded by at least one of a component lead (208), a component body (206), and the printed wiring board (202), wherein each at least one volume of space comprises at least one opening on the surface of the printed circuit board (304); and a layer of non-electrically-conductive filler material (902) adhered to printed circuit board (304) surfaces to provide a contoured, contiguous filler material surface (912), wherein the filler material at least partially infills the at least one volume of space through the at least one opening, and further wherein the filler material bridges across the at least one opening so as to encapsulate and seal the at least one volume of space. *(See,* Applicant's application, pg. 31, ln. 9 to 33, ln. 30.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether the Examiner improperly rejected claims 1, 3, 4, 5, 7, 11, 12, 14 and 15 as being anticipated by U.S. Patent No. 6,127,038 to McCullough ("*McCullough*" herein) when *McCullough* neither discloses, teaches nor suggests "an electrically non-conductive filler material disposed...on the surface of the printed circuit board so as to bridge across the one or more openings of the volume of space...wherein the filler material renders the space substantially inaccessible to subsequently-applied coatings."

2. Whether the Examiner improperly rejected dependent claims 6, 8, 9, 10, 13 and 17 as being unpatentable over *McCullough* in view of JP 200034457A to Kotani *et al.* ("*Kotani*" herein), when neither *McCullough* nor *Kotani* disclose, teach or suggest a filler material as defined in Applicant's independent claims, when the applied art fails to teach or suggest combining the features recited in these claims with Applicant's claimed filler material, and when there is no suggestion or motivation in the applied art to combine the teachings of *McCullough* and *Kotani.*

3. Whether the Examiner improperly rejected dependent claim 16 as being unpatentable over *McCullough* in view of US Patent 5,639,989 to Higgins III ("*Higgins*" herein), when neither *McCullough* nor *Higgins* disclose, teach or suggest a filler material as defined in Applicant's independent claims, when the applied art fails to teach or suggest

combining the features recited in these claims with Applicant's claimed filler material, when the applied art fails to teach or suggest combining the features recited in this claim with Applicant's claimed filler material, and when there is no suggestion or motivation in the applied art to combine the teachings of *McCullough* and *Higgins*.

VII. ARGUMENT

The following arguments address various combinations of the above groups of claims based on the similarity of the rejections levied by the Examiner and/or by the similarity of the Applicant's basis for traversing such rejections.

A. Introduction to Disclosed Embodiments of Applicant's Claimed Invention

Embodiments of the present invention are directed to a printed circuit board comprising a printed wiring board with at least one component mounted thereon. In a typical printed circuit board there are relatively small volume of spaces, also referred to as cavities, defined by neighboring components (leads and/or body) and the printed wiring board on which the components are mounted. Such cavities or volumes of space typically have at least one opening on the surface of the printed circuit board. An example of such a volume of space is described in Applicant's application with reference to Figure 9D, reproduced below. As shown in Figure 9D, there are a number of cavities or volumes of space 900A-900C each defined by a combination of the printed wiring board 202, a body of a component 302 and the leads 906 of component 302. The cavities 900 each have at least one opening to the surface of the printed circuit board such as, for example, between neighboring leads. *(See,* Applicant's application, pg. 31, lns. 10-20.)

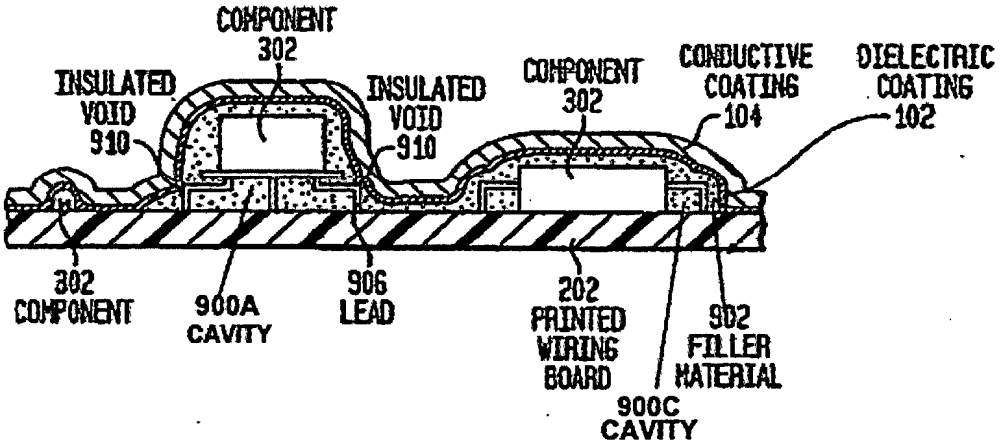


Figure 9D of Applicant's Application

In the exemplary embodiment of Figure 9D, Applicant's claimed filler material is identified by reference numeral 902. Filler material 902 is an electrically non-conductive material which may be extruded on to the surface of the printed circuit board immediately surrounding each cavity 900 so as to bridge across the opening(s) of the cavity to encapsulate and seal the cavity, and to render the cavity substantially inaccessible to subsequently-applied coatings. In the example shown in Applicant's Figure 9D, filler material 902 is disposed over the two illustrated components 302 and the surrounding area of the printed wiring board 202. As noted, filler material 902 bridges across the openings between neighboring leads, as well as the opening between a lead, component body and printed wiring board Oftentimes, cavities 900A-C are also at least partially filled with filler material 902. In the exemplary application illustrated in Figure 9D, cavities 900 are substantially filled with filler material 902 although is this not a requirement of the present invention. *(See,* Applicant's application, pg. 31 to pg. 32, ln. 10.)

As described in Applicant's application, a dielectric coating 102 may be applied to surfaces of the printed circuit board to provide an insulating surface between the printed circuit board and a subsequently-applied conductive coating 104. Without such a prior application of filler material 902, dielectric coating 102 would be directly applied to surfaces of the printed circuit board including surfaces of the printed wiring board and components which bound or define the noted cavities 900. As noted in Applicant's application, because

such surfaces are difficult to access and, therefore, cover, with an applied coating, dielectric coating 102 may not sufficiently coat the cavity surfaces to prevent the subsequently applied conductive coating 104 from forming short-circuit conductive pathways on the printed circuit board. (*See,* Applicant's application, pg. 31, lns. 21-30.)

In contrast, Applicant's claimed printed circuit board comprises Applicant's filler material 902 bridging across the openings of the volumes of space 900, rendering each such volume of space inaccessible to subsequently–applied coatings. As a result, the filler material 902 eliminates the requirement that dielectric coating 102 penetrate the volumes of space 900 to coat component and/or wiring board surfaces which bound and define the volume of space. *(See,* Applicant's application, pg. 32, lns. 11-19.)

In the embodiment described in Applicant's application, filler material 902 is preferably thixotropic, enabling it to be extruded over cavities 900 to cover the top, side and other surfaces of the printed wiring board and components which surround the openings to the cavities 900. In one embodiment, filler material 902 is an epoxy such as any epoxy from the family of Bisphenol-A epoxies mixed with amine hardener. A thermally cured epoxy is preferred due to the inability to directly apply UV radiation to filler material 902 that is disposed in cavities 900 due to shadows cast by components. In other embodiments, filler material 902 is either a latex based non-electrically conductive coating, such as HumiSeal TS300 epoxy, or a gray, two-part epoxy manufactured with glass bead spacers to control the bond line thickness, such as the epoxy ABLEBOND 9349K. *(See,* Applicant's application, pg. 32, 1. 30 to pg. 33, ln. 2.)

B. *McCullough* Neither Discloses, Teaches Nor Suggests Applicant's Filler Material Recited in Independent Claims 1 and 12 Leaving The Office Action Without A *Prima Facie* Rejection

In the Office Action mailed March 11, 2005, the Examiner rejected independent claims 1 and 12 under 35 U.S.C. § 102(e) as being anticipated by *McCullough.* Specifically, the Examiner asserts that *McCullough's* first coating layer 14 bridges across at least one opening of a cavity on a printed circuit board to encapsulate and seal the cavity, and that *McCullough's* first coating layer 14 renders the cavity substantially inaccessible to subsequently-applied coating, thereby anticipating Applicant's invention as recited in

independent claims 1 and 12. (*See*, Office Action, pg. 3.) For at least the reasons provided below, the Examiner's interpretation of *McCullough* is incorrect resulting in an improper rejection that should be reversed.

1. *McCullough's* First Coating Layer 14 Does Not Bridge Across Cavity Openings As Alleged By The Examiner

McCullough is directed to a printed circuit board coating which does not delaminate or crack. *(See, McCullough,* col. 1, lns. 5-10, 33-44.) The *McCullough* conformal coating comprises two layers: a first coating layer 14 directly deposited on printed circuit board surfaces 20, component surfaces 22 and lead surfaces 24, and a second coating layer 16 deposited on first coating 14. Together, layers 14 and 16 provide a continuous, stratified coating which is sealed and corrosion resistant. *(See, McCullough,* col. 3, lns. 8-19.)

A fair reading of *McCullough* clearly shows that *McCullough* fails to support the Examiner's interpretation of *McCullough's* first coating layer 14. In contrast to the Examiner's assertions, the two layers 14, 16 of *McCullough's* coating are separately applied to all surfaces of the printed circuit board, including surfaces that define the walls of cavities on the printed circuit board. This is illustrated in *McCullough's* only figure, Figure 1, which is reproduced to the right. *McCullough's* Figure 1 is a sectional view of a printed circuit board with a single component mounted thereon. *(See, McCullough,* col. 2, lns. 55-58.) There is a cavity or volume of space bounded by surfaces of the component, the component leads and the printed wiring board. As described below, the purpose of *McCullough* is to coat all surfaces of the printed circuit board with coatings 14, 16. Accordingly, as shown in McCullough's Figure 1 above, all component surfaces 22, lead surfaces 24 and printed circuit board surfaces 20 that bound and define the noted cavity, are coated by layer 14, as shown in *McCullough's* Figure 1. *(See, McCullough,* col. 2, lns. 35-43; col. 3, lns. 2-5.).

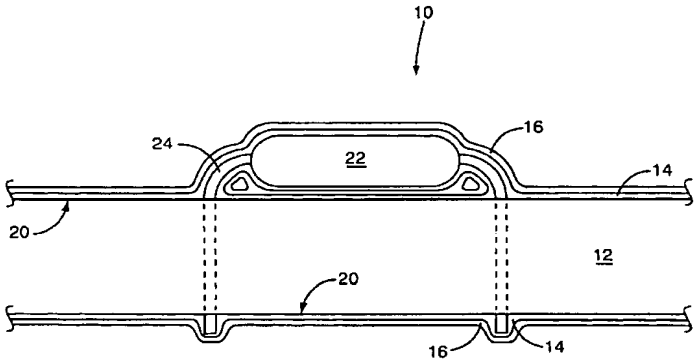


Figure 1 of McCullough

This is further illustrated in the following three figures, which are modified versions of *McCullough's* Figure 1 above. Figure 2A, which is shown below, is *McCullough's* Figure 1 modified to remove coating layers 14, 16 thereby showing the printed circuit board prior to application of *McCullough's* coating layers. As shown by reference numeral 900, there is a volume or space, or cavity, between surface 20 of printed wiring board 12 and the leads 24 and the body of component 22. As described in *McCullough* and a is customary, volume of space 900 is accessible to subsequently applied coatings 14, 16 applied to the printed circuit board 10.

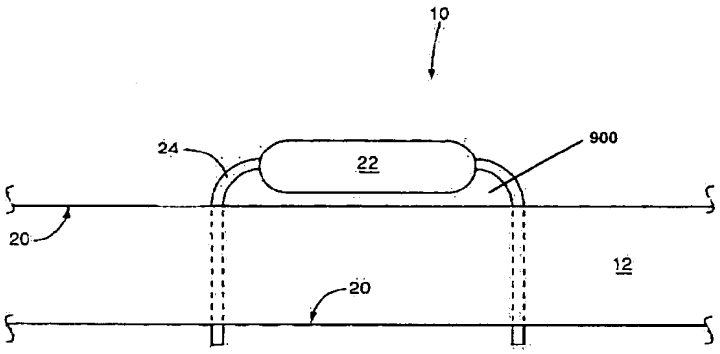


Figure 2A (McCullough's Figure 1 (modified))

Figure 2B, which is shown to the right, is *McCullough's* Figure 1 modified to remove coating layer 16 thereby showing the printed circuit board subsequent to application of coating layer 14, and prior to application of *McCullough's* coating layer 16. As shown, coating layer 14 coats all surfaces of the printed wiring board 12 and component 22, including those surfaces which define volume of space 900, reducing the size of volume of space 900. As discussed elsewhere herein, volume of space 900, albeit smaller in volume due to the presence of layer 14, is still accessible to subsequently applied coatings as illustrated in

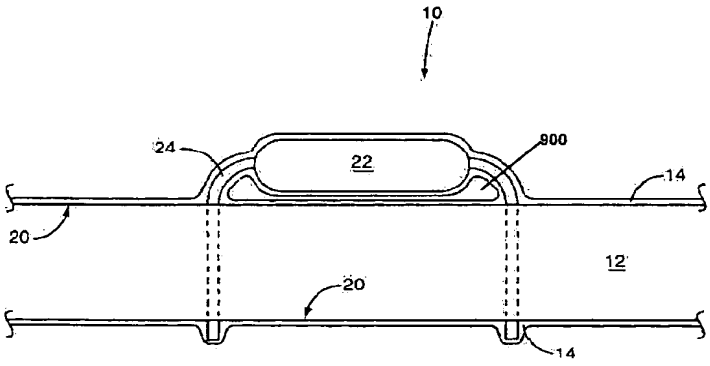


Figure 2B (McCullough's Figure 1 (modified))

Figure 2B. In other words, just as prior to the application of coating layer 14, as shown in Figure 2A, there is nothing obstructing the openings of volume of space 900 on the surface of printed circuit board 10. Such openings, albeit smaller due to the presences of coating layer 14, remain open to provide access to volume of space 900 to subsequently applied coatings.

This is shown in Figure 2C, which is *McCullough's* Figure 1 modified to show the printed circuit board subsequent to application of *McCullough's* coating layers 14 and 16. As shown, coating layer 16 coats coating layer 14, including coating layer 14 applied to the surfaces of printed wiring board 12 and component 22 which define volume of space 900. Thus, in contrast to the Examiner's assertions, coating layer 14 fails to prevent coating layer 16 from being applied to surfaces of printed circuit board 10 which define volume of space 900.

In fact, as shown in Figure 2C, which is shown to the right, volume of space 900 continues to be present to receive additional coatings. The portion of volume of space 900 located between the body of component 22 and printed wiring board surface 20 has been filled in by coating layers 14, 16. However, the portion of volume of space 900 bounded by the surfaces of the leads 24 and body of component 22 and printed wiring board surface 20, albeit reduced in volume due to the presence of coating layers 14, 16, is still present and accessible.

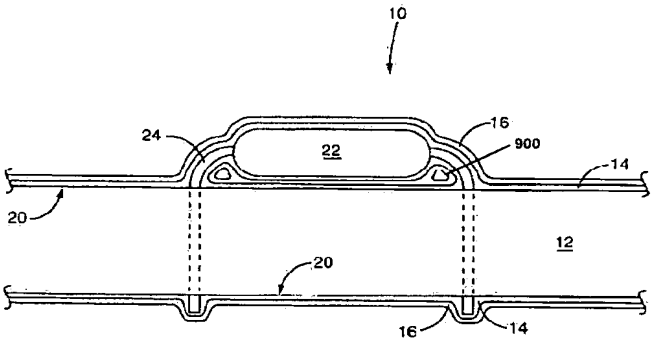


***Figure 2C (McCullough's* Figure 1 (modified))**

Nowhere does *McCullough* disclose, teach or suggest that first coating layer 14 bridge across a cavity opening as recited in Applicant's independent claims 1 and 12. Rather, *McCullough's* first coating layer 14 is deposited on printed circuit board surfaces [Figure 2B above] to prepare the surfaces for the second coating layer 16, which is "deposited onto the first coating layer 14 [Figure 2C above], thereby providing a continuous, conformal stratified coating 14, 16 ..." (*See*, *McCullough*, col. 3, lns. 15-17; emphasis added.)

2. The Examiner Has Continued To Rely On Specific Teachings of McCullough Which Do Not Support The Examiner's Interpretation of *McCullough's* Disclosure

The Examiner has continued to rely on the following teachings of *McCullough* in support of the above rejections.

> After cleaning, *a first coating layer 14 is deposited on most, and preferably all, of the printed circuit board surfaces 20, component surface 22 and lead surfaces 24 that may be potentially exposed to air, moisture or water.* Although depositing the first coating layer 14 on all surfaces may be impractical or impossible, efforts should be made to maximize coverage. Board cleaning and coating compositions are discussed in detail below.
>
> ...
>
> In the preferred embodiment, the first coating layer comprises a material generally selected from the group consisting of parylene, urethane, acrylic, epoxy, and silicone-based resins. Most preferably, the first coating layer comprises parylene, which provides a bonded coating that will not delaminate from the printed circuit board or parts mounted thereto. The chemical composition of parylene is $C_{16}H_{14}C_{12}$. Furthermore, the use of parylene allows for board repair, via partial coating removal and redeposition, as necessary. *The first coating 14 is preferably vacuum deposited on the ultra-clean circuit board and components mounted thereon to maximize coverage of board, component and lead surfaces while providing uniform deposition.*
>
> (*See*, *McCullough*, col. 3, lns. 8-15; lns. 52-64. Emphasis added.)

The above and other portions of *McCullough* fail to support the Examiner's interpretation of *McCullough's* first coating layer 14. The first excerpt teaches that first coating layer 14 is deposited on most if not all printed circuit board surfaces potentially exposed to air, moisture or water. *McCullough* expressly states that such surfaces include surfaces 20 of the board, surfaces 22 of components and surfaces 24 of component leads. Thus, this portion of *McCullough* teaches that *McCullough's* first coating layer 14 coats all surfaces including those that define cavities in the printed circuit board; it does not teach or suggest that first coating layer 14 bridges across cavity openings so as to render the cavity substantially inaccessible to *McCullough's* second coating layer 16. Nor does this or any

other portion of *McCullough* teach or suggest that first coating layer 14 bridges across cavity openings to encapsulate and seal the cavity.

The second excerpt teaches the type of materials that can be used for first coating layer 14 to provide a bonded coating that will not delaminate, and that the first coating layer 14 is preferably vacuum deposited to maximize coverage of board, component and lead surfaces. This teaching also fails to teach or suggest Applicant's filler material as recited in independent claims 1 and 12.

For at least these reasons, Applicant respectfully asserts that the Examiner has misapprehended the teachings of *McCullough*, resulting in an improper rejection of Applicant's claims 1 and 12. Accordingly, Applicant respectfully asserts that the Section 102 rejections of claims 1 and 12 be reversed.

3. *McCullough* Teaches Away From Applicant's Claimed Filler Material

Furthermore, if, as the Examiner maintains, *McCullough's* first coating layer 14 bridged across openings into the noted volume of space to encapsulate and seal the volume of space (as recited in Applicant's independent claim 12), or otherwise rendered the volume of space substantially inaccessible to subsequently-applied coatings (as recited in Applicant's independent claim 1), *McCullough's* first coating layer 14 would prevent *McCullough's* second coating layer 16 from being deposited on the first coating layer 14, directly contradicting the teachings of *McCullough*.

Specifically, if *McCullough's* first coating layer 14 prevented *McCullough's* second coating layer 16 from coating the surfaces of first coating layer 14, as the Examiner suggests, then *McCullough* could not contain a "second coating layer 16 that is deposited onto the first coating layer 14, thereby providing a continuous, conformal, stratified coating 14, 16 which is sealed and corrosion resistant over the surface of the board, components and respective leads," as described by *McCullough*. (*See*, *McCullough*, col. 3, lns. 8-19; emphasis added.) That is, were *McCullough's* first coating layer 14 to function as alleged by the Examiner, *McCullough's* coating layer 14 would fail to achieve the stated purpose of *McCullough* to provide a conformal coating comprised of two coating layers 14, 16 applied to all exposed surfaces on the printed circuit board including surfaces of the components and leads,

including between and behind lead surfaces. (*See*, *McCullough*, col. 2, lns. 19-31; col. 3, lns. 8-11; lns. 61-64; emphasis added.) Therefore, *McCullough's* first coating layer 14 does not, and in fact must not, bridge across openings on the surface of the printed circuit board so to encapsulate and seal the spaces (as recited in Applicant's claim 12), nor render the spaces substantially inaccessible to subsequently-applied coating (as recited in Applicant's claim 1). Thus, rather than teaching or suggesting Applicant's invention as recited in claims 1 and 12, *McCullough* teaches away from Applicant's claimed invention.

For at least the above reasons, Applicant respectfully asserts that the Examiner has failed to meet his burden of providing a reference that either expressly or inherently teaches each of the elements of the Applicant's independent claims 1 and 12. Accordingly, Applicant respectfully asserts that the Section 102 rejection of independent claims 1 and 12 should be reversed.

C. The Examiner's Reasoning In Making The Obviousness Rejection Of Dependent Claims 6, 8-10, 13 and 17 Is Incorrect, Leaving The Office Action Without A *Prima Facie* Rejection

Claims 6, 8-10, 13 and 17 stand rejected under 35 USC 103(a) as being unpatentable over *McCullough* in view of Japanese Patent No. JP 200034457 A to Kotani *et al.* (hereinafter, "*Kotani*"). Specifically, The Examiner acknowledges that *McCullough* fails to disclose a filler material that is thixotropic or a thermally cured epoxy. The Examiner relies on *Kotani* for such a teaching, alleging that "it would have been obvious to one having ordinary skill in the art at the time of the invention was made to employ thixotropic epoxy resin including a thermally cured epoxy in the PCB of *McCullough*, as taught by *Kotani* for the purpose of retaining a sufficient adhesion thickness under high bearing pressure and maintaining a strength at temperature that [is] applied on the surface of the PCB" (*See*, Office Action para. 7, pg. 5.)

An Examiner may only establish a *prima facie* case of obviousness when "the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993). In asserting that the prior art "suggested" the claimed subject matter, an Examiner may not "use the claimed invention as an instruction manual or 'template' to

piece together the teachings of the prior art so that the claimed invention is rendered obvious." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). The Federal Circuit has further stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." Id. Here, the Examiner has selected features from different references in an attempt to construct a *prima facie* obviousness rejection. This is impermissible hindsight reconstruction of Applicant's invention.

McCullough's first coating layer 14 is "preferably vacuum deposited on the ultra-clean circuit board and components mounted thereon to maximize coverage of board, component, and lead surfaces while providing uniform deposition." (*See*, *McCullough*, col. 3, lns. 61-64.) *Kotani* teaches a high-pressure proof thixotropic epoxy resin adhesive for adhesion of precast concrete which is subjected to high planar pressure at the time of construction. (*See*, *Kotani*, paras. 1, 3, 5 and 6.) There is no teaching or suggestion to utilize *Kotani's* resin adhesive as the first coating layer 14 in *McCullough's* continuous, conformal stratified coating. In fact, due to its characteristically low viscosity when in an un-agitated state, the thixotropic resin of *Kotani* is not suitable for vacuum deposition, *McCullough's* preferred method for applying first coating layer 14.

Furthermore, the motivation suggested by the Examiner, namely, retaining a sufficient adhesion thickness under high bearing pressure and maintaining a strength at temperatures at which the coating is applied, are apparently considerations when mixing and setting concrete, as described in *Kotani.* (*See, Kotani*, para. 5.) Such considerations, however, have not been shown to be relevant to coating printed circuit boards.

Accordingly, Applicant respectfully asserts that such unsupported allegations of motivating factors are not proper motivations to selectively modify or add to the teachings of *McCullough* in an attempt to meet Applicant's novel claimed invention. Thus, the only conclusion that can be drawn, based on the record of this application, is that the suggestion forming the basis for the Examiner's otherwise factually unsupported conclusion must have come from Applicant's own novel disclosure; that is, they are based on impermissible hindsight. This failure of the Examiner's reasoning in attempting to make out a *prima facie* case is sufficient reason alone to reverse the Section 103 rejection of claims 6, 8-10, 13 and 17.

D. The Examiner's Reasoning In Making the Obviousness Rejection Of Dependent Claim 16 Is Incorrect, Leaving The Office Action Without A *Prima Facie* Rejection

Dependent claim 16 stands rejected under 35 USC 103(a) as being unpatentable over *McCullough* in view of U.S. Patent No. 6,127,038 to Higgins (hereinafter, "*Higgins*"). Specifically, the Examiner acknowledges that *McCullough* fails to disclose "a conductive coating covering the dielectric coating and portions of the printed circuit board not covered by the dielectric coating" as recited in Applicant's claim 16. The Examiner relies on *Higgins* for such a teaching, alleging that "it would have been obvious to one having ordinary skill in the art at the time of the invention was made to employ as conductive coating as claimed in the PCB of *McCullough*, as taught by *Higgins*, for the purpose of providing ground shielding potential to the PCB. This is incorrect.

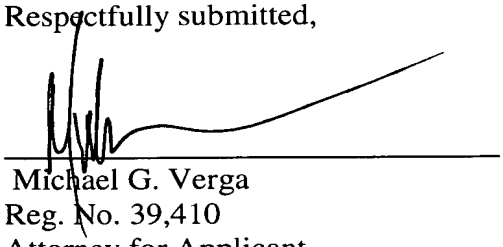
There is no teaching or suggestion in either *McCullough*, *Higgins* or the other art of record to apply the conductive coating of *Higgins* to the dual-layer, stratified coating 14, 16 of *McCullough*. The motivation proposed by the Examiner in support of this rejection, i.e., to provide ground shielding potential to the PCB, is not mentioned as a need or desire in *McCullough* or the other art of record. There is also no teaching or suggestion in the art of record to replace the insulating coating 24 of *Higgins* with the stratified coating 14, 16 of *McCullough*. For example, there is no disclosure of a need or desire to prevent delamination or cracking of *Higgins*' insulating coating 24. Nor is there any other reason that can be derived from the art of record that would suggest such a combination of cited references.

Thus, the only conclusion that can be drawn, based on the record of this application, is that the suggestion forming the basis for the Examiner's otherwise factually unsupported conclusion must have come from Applicant's own novel disclosure; that is, they are based on impermissible hindsight. This failure of the Examiner's reasoning in attempting to make out a *prima facie* case is sufficient reason alone to reverse the Section 103 rejection of claim 16.

D. Conclusion

For the reasons noted above, Applicant submits that the pending claims define patentable subject matter. Accordingly, Applicant request that the Examiner's rejection of these claims be reversed and that the pending application be passed to issue.

Respectfully submitted,



Dated: December 20, 2006

Michael G. Verga
Reg. No. 39,410
Attorney for Applicant

CLAIMS APPENDIX

1. A printed circuit board comprising:

a printed wiring board;

a component mounted on the printed wiring board, wherein the printed circuit board has a volume of space bounded by at least one of a body of the component, a lead of the component, and said printed wiring board, wherein said volume of space has at least one opening on the surface of the printed circuit board; and

an electrically non-conductive filler material disposed on the surface of the printed circuit board so as to bridge across the at least one opening of the volume of space to render the volume of space substantially inaccessible to subsequently-applied coatings.

3. The printed circuit board of claim 1, wherein the volume of space is bounded by leads of said component, a body of said component, and said printed wiring board, wherein at least one of the at least one opening on the surface of the printed circuit board is located between neighboring component leads

4. The printed circuit board of claim 1, wherein the component is one of a plurality of components, and wherein the volume of space is bounded by at least two or more of the plurality of components.

5. The printed circuit board of claim 1, wherein the volume of space is bounded by the component and the printed wiring board.

6. The printed circuit board of claim 1, wherein said filler material is thixotropic.

7. The printed circuit board of claim 1, wherein said filler material is an epoxy.

8. The printed circuit board of claim 7, wherein said epoxy is one of the family of Bisphenol-A epoxies mixed with an amine hardener.

9. The printed circuit board of claim 7, wherein said epoxy is a thermally cured epoxy.

10. The printed circuit board of claim 7, wherein said epoxy is a latex based non-electrically conductive epoxy.

11. The printed circuit board of claim 1, wherein the subsequently-applied coating comprises:

a layer of dielectric coating that conformingly coats exposed surfaces of the printed wiring board, the component, and the filler material, wherein the at least one opening of the volume of space is sufficiently large to prevent the dielectric coating from bridging across the at least one opening without the presence of the filler material.

12. A printed circuit board comprising:

a printed wiring board;

a plurality of components each mounted on said printed wiring board, wherein the printed circuit board has at least one volume of space bounded by at least one of a component lead, a component body, and the printed wiring board, wherein each at least one volume of space comprises at least one opening on the surface of the printed circuit board; and

a layer of non-electrically-conductive filler material adhered to printed circuit board surfaces to provide a contoured, contiguous filler material surface, wherein the filler material at least partially infills the at least one volume of space through the at least one opening, and further wherein the filler material bridges across the at least one opening so as to encapsulate and seal the at least one volume of space.

13. The printed circuit board of claim 12, wherein said filler material is thixotropic.

14. The printed circuit board of claim 12, wherein said filler material is an epoxy.

15. The printed circuit board of claim 14, further comprising:

a low viscosity, high adherence dielectric coating that, when applied and cured, covers portions of said printed circuit board coated with the filler material, wherein the filler material prevents the dielectric coating from entering the at least one opening of the at least one volume of space.

16. The printed circuit board of claim 15, further comprising:

a conductive coating covering at least a portion of said dielectric coating, wherein the dielectric coating and the conductive coating form a conformal electromagnetic interface (EMI) shield that adheres to and conforms with the printed circuit board surfaces.

17. The printed circuit board of claim 14, wherein said filler material is thixotropic.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None